SD56120

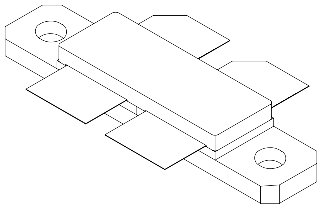
RF POWER Transistors, LDMOST plastic family
N-Channel enhancement-mode lateral MOSFETs

General features

- Excellent thermal stability
- Common source configuration Push-pull
- P_{OUT} = 100W with 14dB gain @ 860MHz
- BeO free package

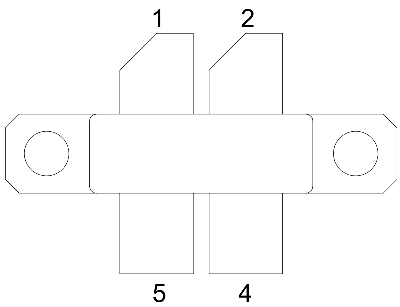
Description

The SD56120 is a common source N-Channel enhancement-mode lateral Field-Effect RF power transistor designed for broadband commercial and industrial applications at frequencies up to 1.0GHz. The SD56120 is designed for high gain and broadband performance operating in common source mode at 28 V. It is ideal for broadcast applications from 470 to 860 MHz requiring high linearity.



M246
Epoxy sealed

Pin connection



1-2 Drain
3 Source
4-5 Gate

Order codes

Part number	Package	Branding
SD56120	M246	TSD56120

Contents

1 Electrical data

1.1 Maximum ratings

Table 1. Absolute maximum ratings (T_{CASE} = 25°C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source Voltage	65	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Drain Current	14	A
P_{DISS}	Power Dissipation (@ Tc = 70°C)	217	W
T_J	Max. Operating Junction Temperature	200	°C
T_{STG}	Storage Temperature	-65 to +150	°C

1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	0.6	°C/W

2 Electrical characteristics

T_{CASE} = +25 °C

2.1 Static

Table 3. Static (per section)

Symbol	Test conditions			Min	Typ	Max	Unit
$V_{(BR)DSS}$	V_{GS} = 0 V	I_{DS} = 1 mA		65			V
I_{DSS}	V_{GS} = 0 V	V_{DS} = 28 V				1	µA
I_{GSS}	V_{GS} = 20 V	V_{DS} = 0 V				1	µA
$V_{GS(Q)}$	V_{DS} = 28 V	I_D = 200 mA		3.0		5.0	V
$V_{DS(ON)}$	V_{GS} = 10 V	I_D = 3 A			0.7	0.8	V
G_{FS}	V_{DS} = 10 V	I_D = 3 A			3		mho
C_{ISS}	V_{GS} = 0 V	V_{DS} = 28 V	f = 1 MHz		82		pF
C_{OSS}	V_{GS} = 0 V	V_{DS} = 28 V	f = 1 MHz		48		pF
C_{RSS}	V_{GS} = 0 V	V_{DS} = 28 V	f = 1 MHz		2.8		pF

Note: REF. 7194566A

2.2 Dynamic

Table 4. Dynamic

Symbol	Test conditions	Min	Typ	Max	Unit
P_{OUT}	V_{DD} = 28 V I_{DQ} = 400 mA f = 860 MHz	100			W
G_{PS}	V_{DD} = 28 V I_{DQ} = 400 mA P_{OUT} = 100 W f = 860 MHz	14	16		dB
η_D	V_{DD} = 28 V I_{DQ} = 400 mA P_{OUT} = 100 W f = 860 MHz	50	60		%
G_{PS}	V_{DD} = 28 V I_{DQ} = 400 mA P_{OUT} = 100 W PEP		16		dB
h_D	V_{DD} = 28 V I_{DQ} = 400 mA P_{OUT} = 100 W PEP		50		%
IMD	V_{DD} = 28 V I_{DQ} = 400 mA P_{OUT} = 100 W PEP		-28		dB_t
Load mismatch	V_{DD} = 28 V I_{DQ} = 400 mA P_{OUT} = 100 W f = 860 MHz All phase angles	5:1			VSWR

Note: f1 = 860 MHz
PEP f2 = 860.1 MHz

3 Impedances

Figure 1. Current conventions

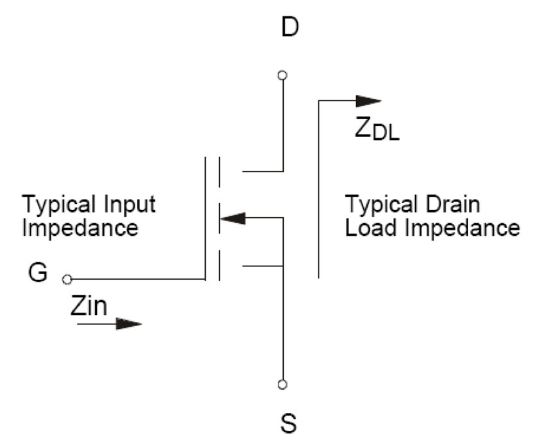


Table 5. Impedance data

Freq. (MHz)	Z_{IN} (Ω)	Z_{DL}(Ω)
860 MHz	1.11 - j 2.63	3.01 + j 5.34

Note: Measured drain to drain and gate to gate respectively.

4 Typical performance

Figure 2. Capacitance vs drain voltage (per section)

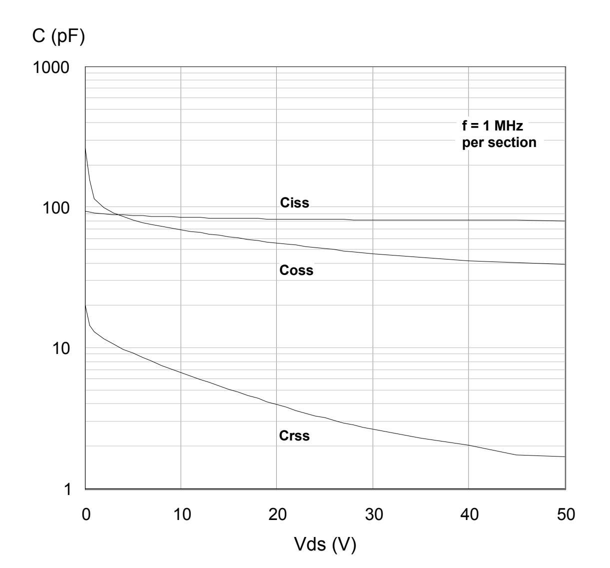


Figure 3. Gate-source voltage vs case temperature

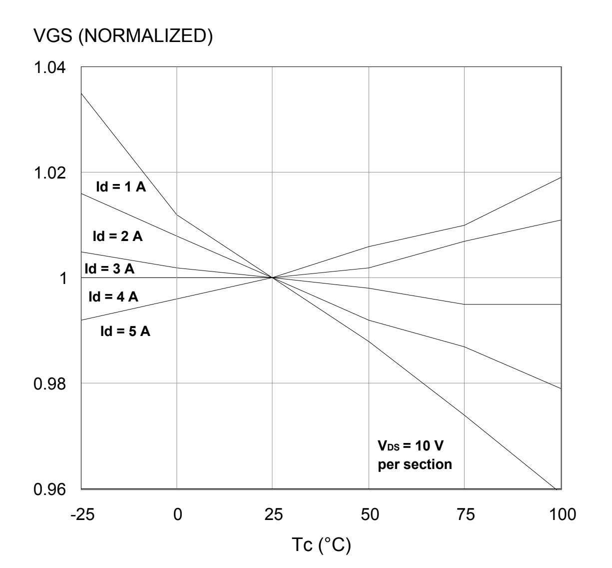


Figure 4. Drain current vs gate voltage

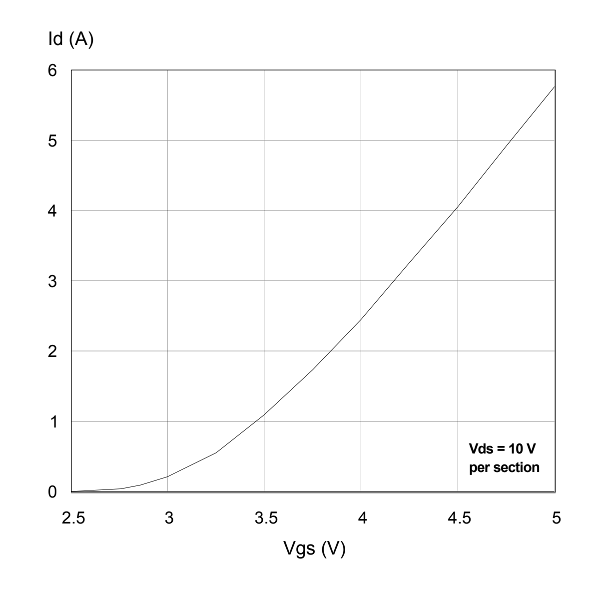


Figure 5. Output power vs input power

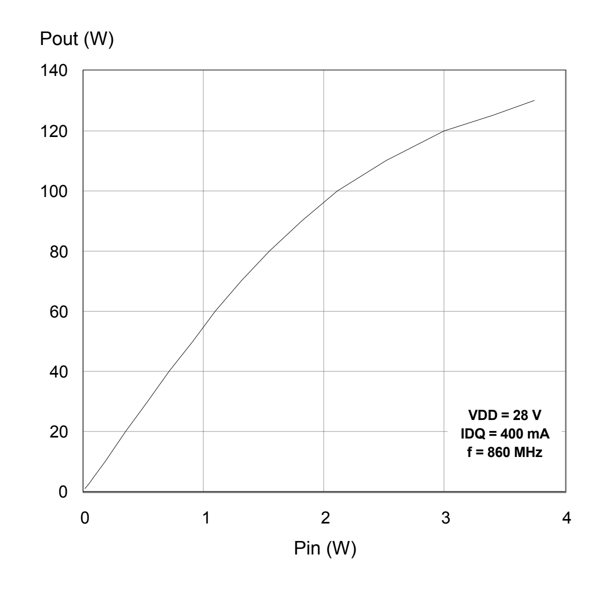


Figure 6. Power gain vs input power

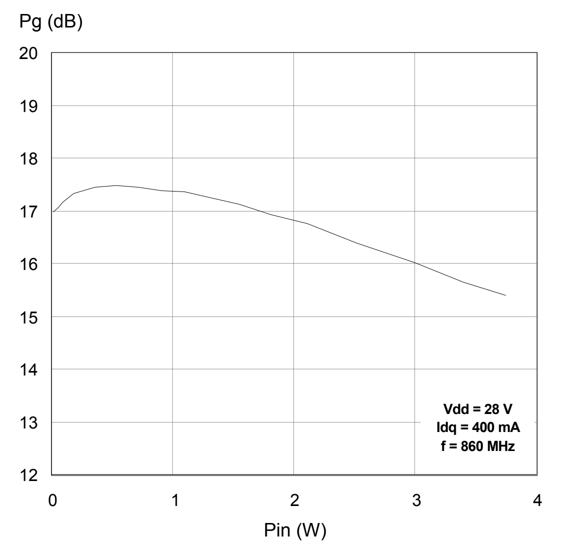


Figure 7. Efficiency vs output power

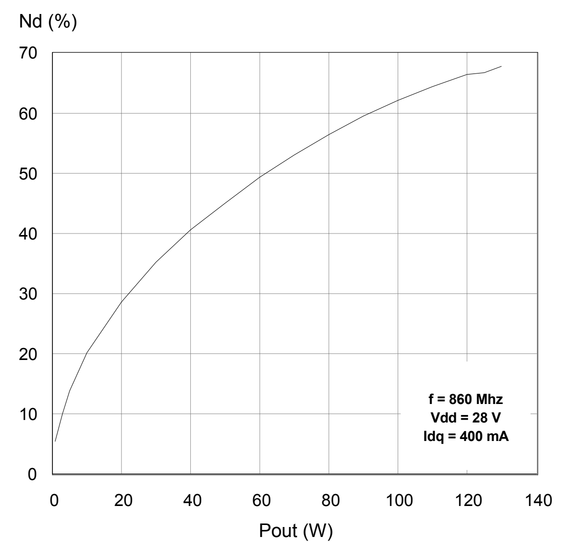


Figure 8. Power gain vs output power

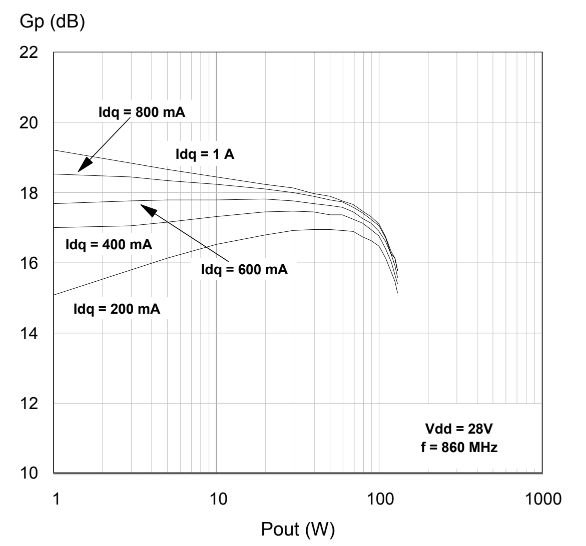


Figure 9. Intermodulation distortion vs output power

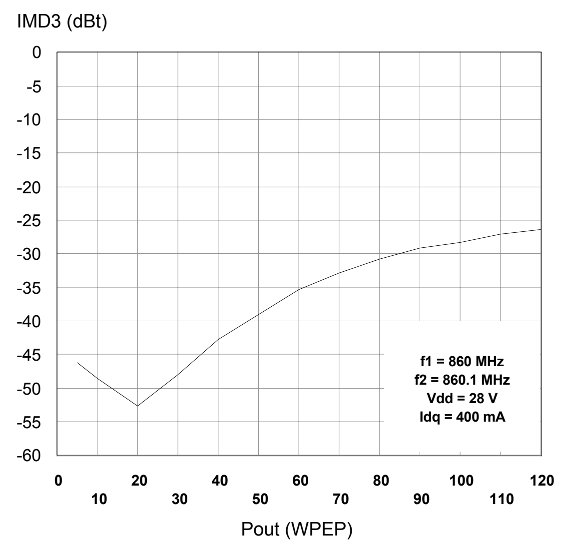


Figure 10. Output power vs drain voltage

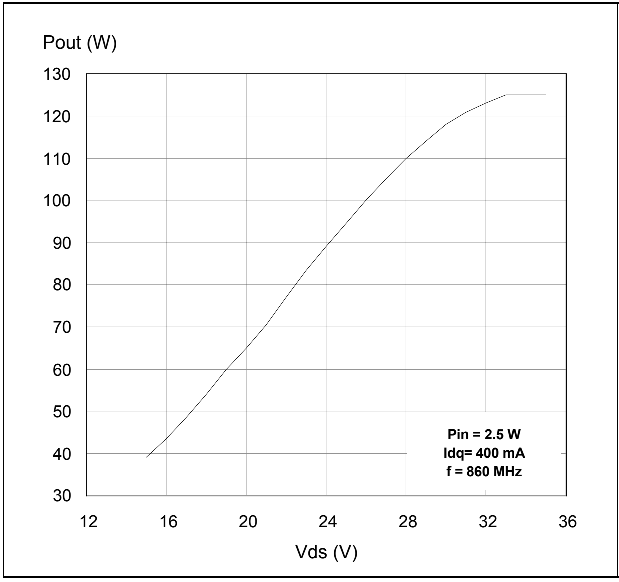


Figure 11. Output power vs bias current

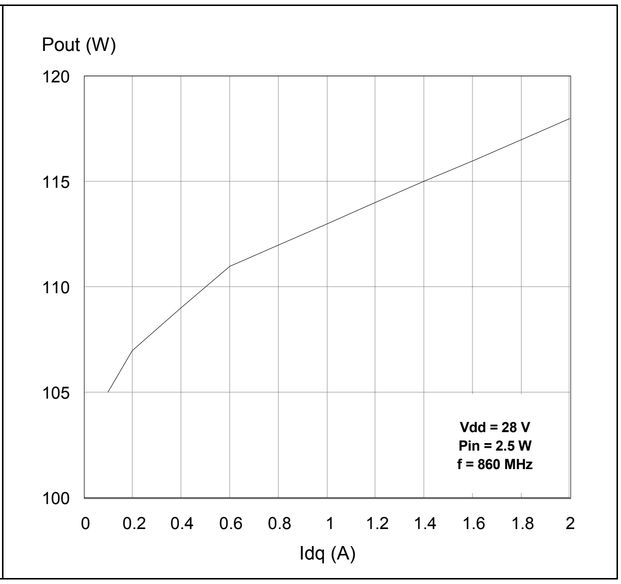
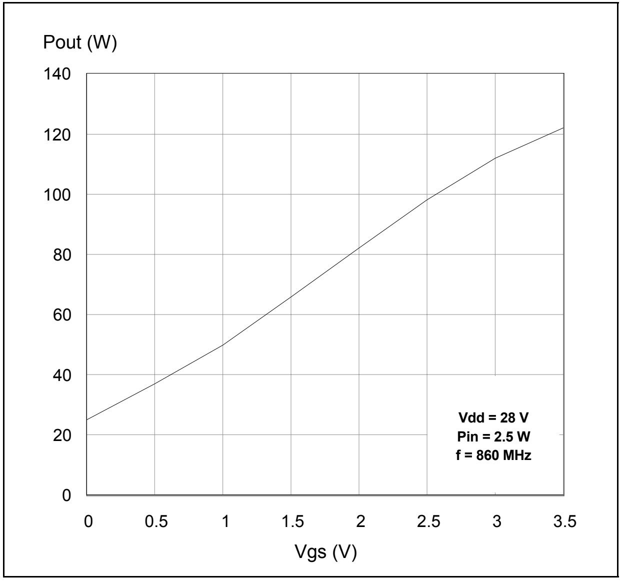
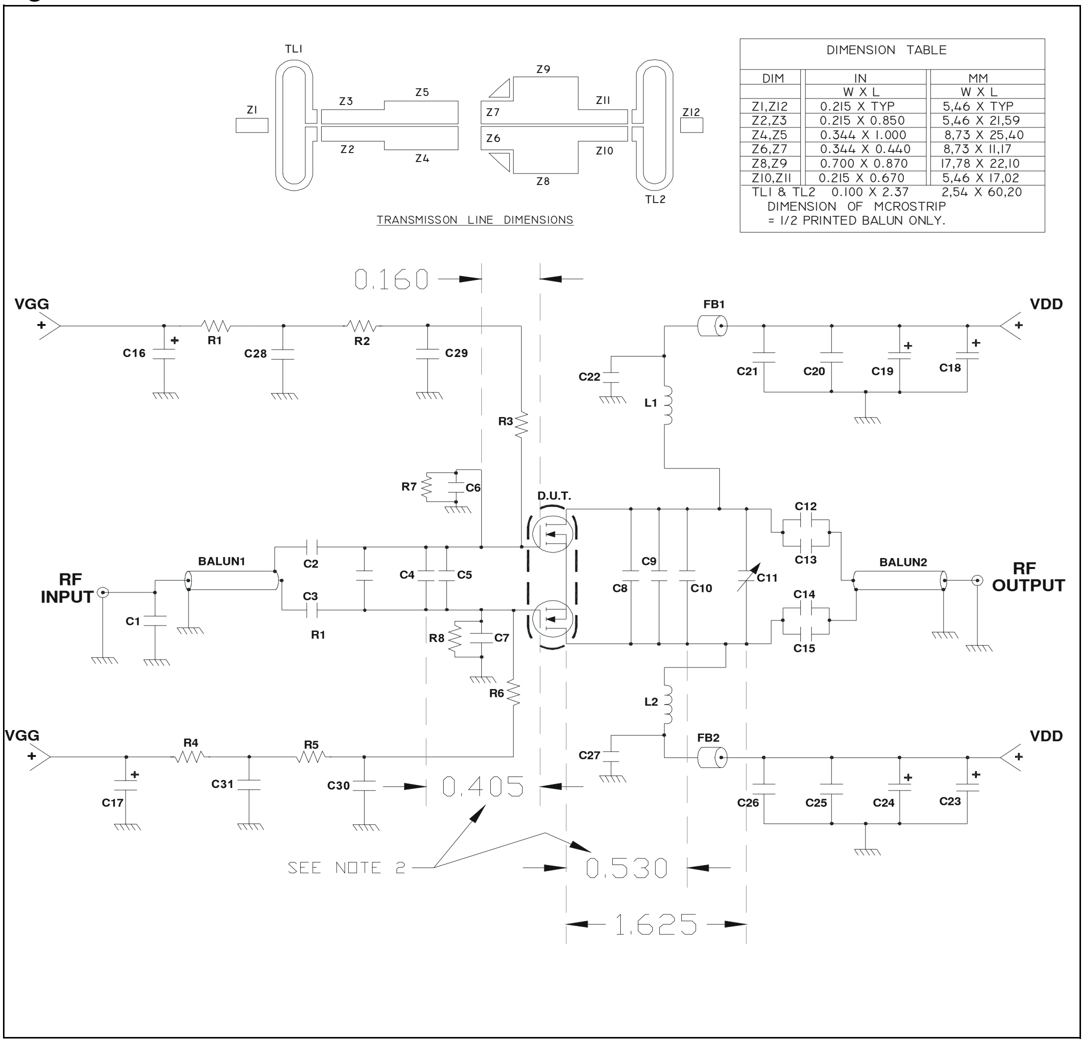


Figure 12. Output power vs gate-source voltage



5 Test circuit

Figure 13. 860MHz test circuit schematic



DIMENSION TABLE		
DIM	IN	MM
	W X L	W X L
Z1,Z12	0.215 X TYP	5,46 X TYP
Z2,Z3	0.215 X 0.850	5,46 X 21,59
Z4,Z5	0.344 X 1.000	8,73 X 25,40
Z6,Z7	0.344 X 0.440	8,73 X 11,17
Z8,Z9	0.700 X 0.870	17,78 X 22,10
Z10,Z11	0.215 X 0.670	5,46 X 17,02
TL1 & TL2	0.100 X 2.37	2,54 X 60,20

DIMENSION OF MCROSTRIP = 1/2 PRINTED BALUN ONLY.

Note: 1 Dimensions at component symbols are reference for component placement.

2 Gap between ground & transmission line = 0.056 [1.42] +0.002 [0.05] -0.000 [0.00] typ.

Table 6. 860MHz test circuit component part list

Component	Description
C32	.6 - 4.5 pF VARIABLE CAPACITOR
C31, C28	.01 µF ATC 200B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C29, C30	62 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C27, C22	270 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C26, C21	1200 pF ATC 700B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C25 ,C20	0.1 µF 500V SURFACE MOUNT CERAMIC CHIP CAPACITOR
C24, C19, C17, C16	10 µF 50V ALUMINUM ELECTROLYTIC RADIAL LEAD SURFACE MOUNT CAPACITOR
C23, C18	100 µF 63V ALUMINUM ELECTROLYTIC RADIAL LEAD CAPACITOR
C15, C14, C13, C12	47 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C11	0.8 - 8 pF GIGATRIM VARIABLE CAPACITOR
C10	3.0 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C9, C8	4.3 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C7, C6, C5	10 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C4	2.0 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C3, C2	20 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C1	1.3 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
R7, R8	100 OHM 1/4 W SURFACE MOUNT CHIP RESISTOR
R6, R3	22 OHM 1/4 W CARBON LEADED RESISTOR
R5, R2	4.7 OHM 1/4 W CARBON LEADED RESISTOR
R4, R1	82 OHM 1/4 W CARBON LEADED RESISTOR
B2, B1	BALUN, 50 OHM SUCOFORM, OD 0.141 2.37 LG COAXIAL CABLE OR EQUIVALENT
L2, L1	INDUCTOR, 6 TURN AIR-WOUND #18AWG ID=0.130[3,30] MAGNET WIRE
FB2, FB1	SURFACE MOUNT EMI SHIELD BEAD
PCB	ULTRALAM 2000. 0.030” THK εr = 2.55, 2 Oz ED CU BOTH SIDES

Figure 14. 860MHz production test fixture

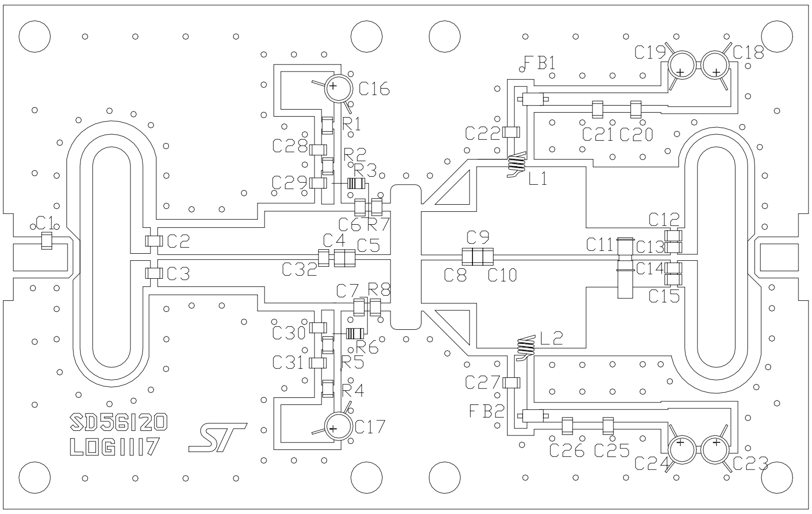
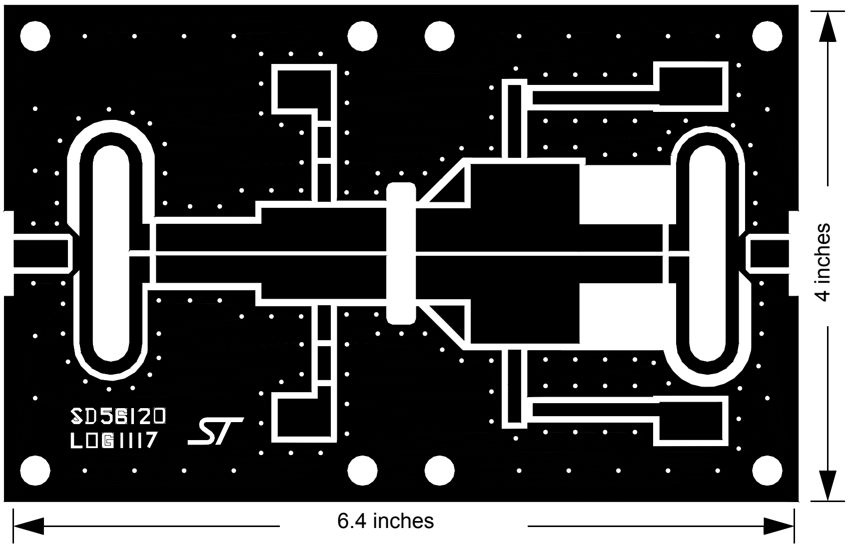


Figure 15. 860MHz test circuit photomaster



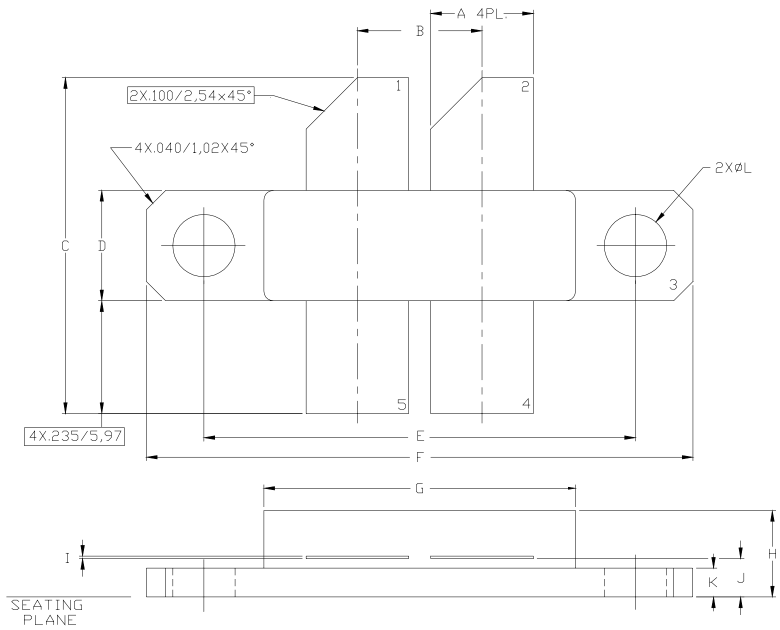
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 7. M246 (.230 x .650 WIDE 4/L BAL N/HERM W/FLG) mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	5.33		5.59	.210		.220
B	6.48		6.73	.255		.265
C	17.27		18.29	.680		.720
D	5.72		5.97	.225		.235
E		22.86			.900	
F	28.83		29.08	1.135		1.145
G	16.26		16.76	.640		.660
H	4.19		5.08	.165		.200
I	0.08		0.15	.003		.006
J	1.83		2.24	.072		.088
K	1.40		1.65	.055		.065
L	3.18		3.43	.125		.135

Figure 16. Package dimensions



Controlling dimension: Inches

Ref. 7145054A

7 Revision history

Table 8. Revision history

Date	Revision	Changes
18-Jun-2001	1	First Issue
12-Sep-2004	2	Few updates
13-Jul-2006	3	New template, added lead free info